What is claimed is:

1. A method of forming a gate contact in a MOSFET device, the steps comprising:

forming a first dielectric layer on a substrate, having oxide-filled isolation trenches, gate structure, sidewall passivation around gate, source and drain with lightly and heavily doped regions;

planarizing said first dielectric layer and recessing said first dielectric layer below the level of said gate structure;

forming a second dielectric etch stop layer over said first dielectric layer;

planarizing said second dielectric layer in level with the gate structure;

pattern said second dielectric layer, using oversize gate mask to leave said second dielectric layer around said gate structure; and

forming electrical gate contact steps comprising: forming an inter-level dielectric layer over partially formed MOSFET device; patterning contact holes to source drain regions, patterning contact hole to gate stopping on said second dielectric layer; forming planarized metal patterns in and over said contact holes.

2. The method of forming a gate contact in a MOSFET device according to claim 1 wherein, said first dielectric layer comprises silicon dioxide, nitridized silicon dioxide, silicon oxy-fluoride, and/or tetraethylorthosilicate.

3. The method of forming a gate contact in a MOSFET device according to claim **2** wherein, said first dielectric layer thickness is approximately between about 1000 °A and 3000 °A after planarization.

4. The method of forming a gate contact in a MOSFET device according to claim **1** wherein, said first dielectric layer is planarized with steps comprising plasma etch back and/or chemical mechanical polishing.

5. The method of forming a gate contact in a MOSFET device according to claim **1** wherein, said first dielectric layer is recessed approximately between about 500 °A and 1000 °A.

6. The method of forming a gate contact in a MOSFET device according to claim **1** wherein, said second dielectric etch-stop layer comprises silicon nitride, oxygen doped silicon nitride, and/or silicon oxy-nitride.

7. The method of forming a gate contact in a MOSFET device according to claim **6** wherein, said second dielectric etch-stop layer thickness is approximately between about 500 °A and 1000 °A after planarization process.

8. The method of forming a gate contact in a MOSFET device according to claim **1** wherein, said second dielectric etch stop layer is planarized with steps comprising plasma etch

back and/or chemical mechanical polishing.

9. The method of forming a gate contact in a MOSFET device according to claim **1** wherein, said inter-level dielectric layer comprises tetraethylorthosilicate, borosilicate glass and/or phosphorous silicate glass.

10. The method of forming a gate contact in a MOSFET device according to claim **9** wherein, said inter-level dielectric layer thickness is approximately between about 8,000 °A and 15,000 °A.

11. A method of forming a poly-silicon gate contact in a MOSFET device, the steps comprising:

forming a silicon dioxide layer on a silicon substrate having oxide-filled isolation trenches, gate structure, sidewall passivation around gate, source and drain with lightly and heavily doped regions;

planarizing said silicon dioxide layer and recessing said silicon dioxide layer below the level of said poly-silicon gate structure;

forming a silicon nitride etch stop layer over said silicon dioxide layer;

planarizing said silicon nitride etch stop layer in level with the gate structure;

pattern said silicon nitride etch stop layer, using oversize poly-silicon gate mask to leave said silicon nitride layer around said poly-silicon gate structure; and

forming electrical poly-silicon gate contact steps comprising: forming an inter-level dielectric layer over partially formed MOSFET device; patterning contact holes to source drain regions, patterning contact hole to poly-silicon gate stopping on said silicon nitride etch stop layer; forming planarized metal patterns in and over said contact holes.

12. The method of forming a poly-silicon gate contact in a MOSFET device according to claim **11** wherein, said post-planarized silicon dioxide layer thickness is approximately between about 1000 °A and 3000 °A.

13. The method of forming a poly-silicon gate contact in a MOSFET device according to claim **11** wherein, said silicon dioxide layer is planarized with steps comprising plasma etch back and/or chemical mechanical polishing.

14. The method of forming a poly-silicon gate contact in a MOSFET device according to claim **11** wherein, said silicon dioxide layer is recessed approximately between about 500 °A and 1000 °A.

15. The method of forming a poly-silicon gate contact in a MOSFET device according to claim **11** wherein, said silicon nitride layer thickness is approximately between about 500 °A and 1000 °A after planarization process.

16. The method of forming a poly-silicon gate contact in a MOSFET device according to claim **11** wherein, said silicon nitride layer is planarized with steps comprising plasma etch back and/or chemical mechanical polishing.

17. A MOSFET device structure comprising:

a semiconductor substrate having device elements comprising oxide-filled isolation trenches, gate structure, sidewall passivation around gate, source and drain with lightly and heavily doped regions;

first dielectric layer over said semiconductor substrate;

second dielectric etch stop layer over said first dielectric layer and around said gate structure;

inter-level dielectric layer over said MOSFET device structure; and

metal line, forming an electrical contacting with said gate.

18. A MOSFET device structure according to claim **17** wherein, said first dielectric layer comprises silicon dioxide, nitridized silicon dioxide, silicon oxy-fluoride, and/or tetraethyl-ortho-silicate.

19. The MOSFET device structure according to claim **17** wherein, said first dielectric layer thickness is approximately between about 1000 °A and 3000 °A.

20. The MOSFET device structure according to claim **17** wherein, said second dielectric etch-stop layer comprises silicon nitride, oxygen doped silicon nitride, and/or silicon oxy-nitride.

21. The MOSFET device structure according to claim **17** wherein, said second dielectric etch-stop layer thickness is approximately between about 500 °A and 1000 °A after planarization process.

22. The MOSFET device structure according to claim **17** wherein, said inter-level dielectric layer thickness is approximately between about 8,000 °A and 15,000 °A.